

FEATURES

- 1). Center amplifying gate
- 2). Metal case with ceramic insulator
- 3). Low on-state and switching losses

TYPICAL APPLICATIONS

- 1). AC controllers
- 2). DC and AC motor control
- 3). Controlled rectifiers

$I_{T(AV)}$	1897A
V_{DRM}/V_{RRM}	1900~3000V
I_{TSM}	25.0 KA
I^2t	$3125 \cdot 10^3 A^2S$



THE MAIN PARAMETERS

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	$T_j(^{\circ}C)$	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled, $T_{hs}=55^{\circ}C$ $T_{hs}=60^{\circ}C$	125			1897 1800	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	$V_{DRM} \& V_{RRM}, tp=10ms$ $V_{DSM} \& V_{RSM} = V_{DRM} \& V_{RRM} + 100V$	125	1900		3000	V
I_{DRM} I_{RRM}	Repetitive peak off-state current Repetitive peak reverse current	$V_D = V_{DRM}$ $V_R = V_{RRM}$	125			120	mA
I_{TSM}	Surge on-state current	10ms half sine wave	125			25	KA
I^2t	I^2T for fusing coordination	$V_R = 0.6V_{RRM}$	125			3125	$A^2s \cdot 10^3$
V_{TO}	Threshold voltage		125			1.05	V
r_T	On-state slop resistance		125			0.24	mΩ
V_{TM}	Peak on-state voltage	$I_{TM}=3220A, F=32KN$	125			2.09	V
dv/dt	Critical rate of rise of off-state voltage	$V_{DM}=0.67V_{DRM}$	125			1000	V/μs
di/dt	Critical rate of rise of on-state current	$V_{DM}=67\%V_{DRM}$ to 2000A, Gate pulse $t_r \leq 0.5 \mu s, I_{GM}=1.5A$	125			200	A/μs
I_{rm}	Reverse recovery current	$I_{TM}=1500A, tp=1000 \mu s,$ $di/dt=-20A/\mu s,$ $VR=50V$	125			200	A
t_{rr}	Reverse recovery time					21	μs
Q_{rr}	Recovery charge					2100	μC
I_{GT}	Gate trigger current	$V_A=12V, I_A=1A$	25	40		300	mA
V_{GT}	Gate trigger voltage			0.8		3.0	V
I_H	Holding current	$V_{DM}=67\%V_{DRM}$	125	20		300	mA
V_{GD}	Non-trigger gate voltage			0.3			V
$R_{th(j-h)}$	Thermal resistance Junction to heatsink	At 180° sine, double side cooled Clamping force 32KN				0.017	°C /W
F_m	Mounting force			27		34	KN
T_{stg}	Stored temperature			-40		140	°C
W_t	Weight				850		g
Size	Package box size			160 × 145 × 65			mm

PERFORMANCE CURVES FIGURE

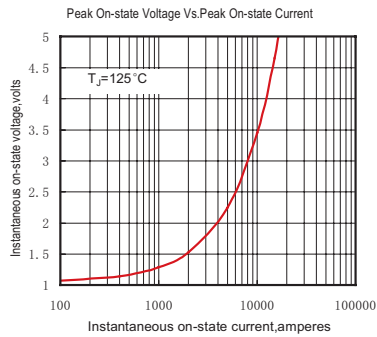


Fig.1

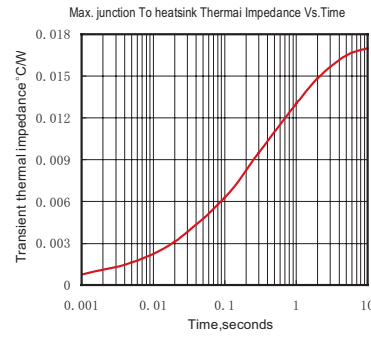


Fig.2

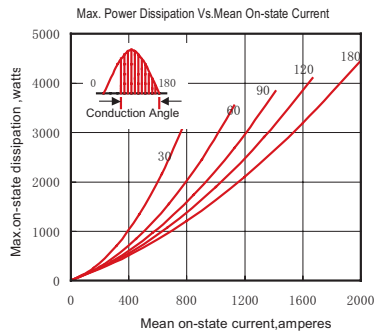


Fig.3

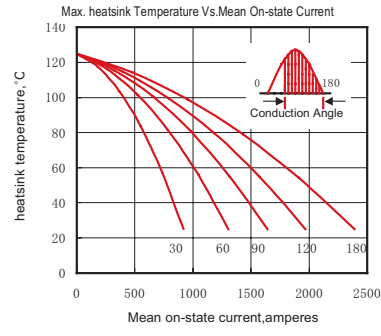


Fig.4

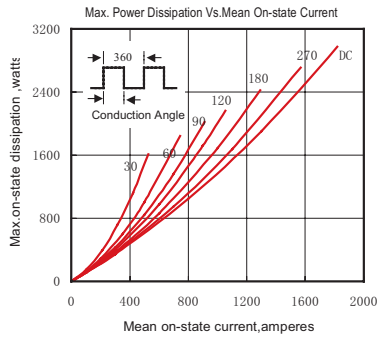


Fig.5

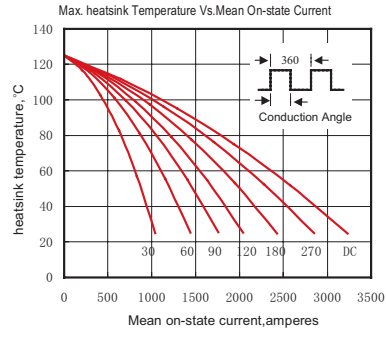


Fig.6

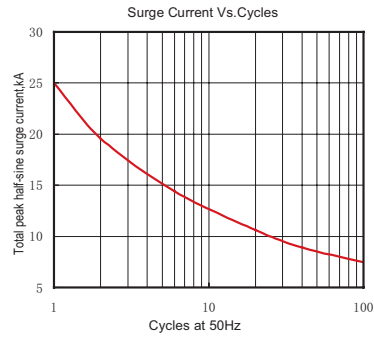


Fig.7

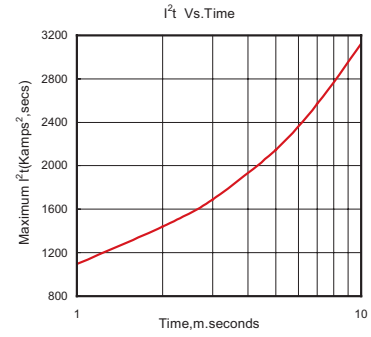


Fig.8

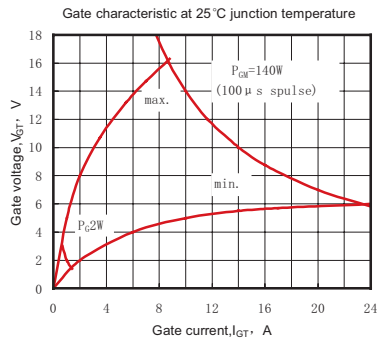


Fig.9

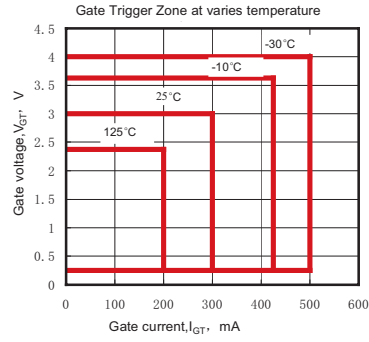
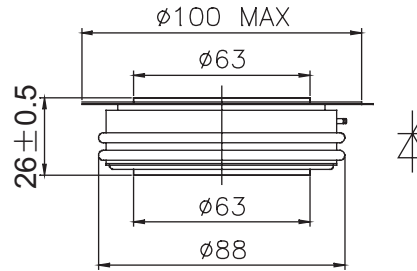
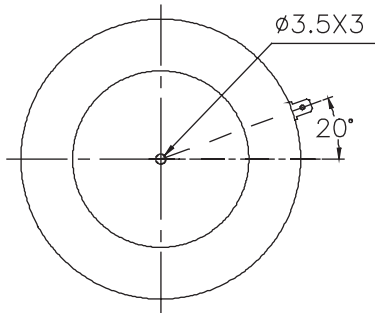


Fig.10

OUTLINE



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