

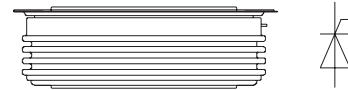
FEATURES

- 1). Center amplifying gate
- 2). Metal case with ceramic insulator
- 3). Low on-state and switching losses

TYPICAL APPLICATIONS

- 1). AC controllers
- 2). DC and AC motor control
- 3). Controlled rectifiers

$I_{T(AV)}$ 3835 A
 V_{DRM}/V_{RRM} 1900-3000V
 I_{TSM} 44 KA
 I^2t 9680 10³A²S



THE MAIN PARAMETERS

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T _J (°C)	VALUE			UNIT
				Min	Type	Max	
I _{T(AV)}	Mean on-state current	180° half sine wave 50Hz Double side cooled, T _{hs} =55°C T _{hs} =64°C	125			3835 3500	A
V _{DRM} V _{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V _{DRM} &V _{RRM} , tp=10ms V _{DSM} &V _{RSM} =V _{DRM} &V _{RRM} +100V	125	1900		3000	V
I _{DRM} I _{RRM}	Repetitive peak off-state current Repetitive peak reverse current	V _D =V _{DRM} V _R =V _{RRM}	125			250	mA
I _{TSM}	Surge on-state current	10ms half sine wave	125			44	KA
I ² t	I ² T for fusing coordination	V _R =0.6V _{RRM}	125			9680	A ² s*10 ³
V _{TO}	Threshold voltage		125			0.99	V
r _T	On-state slop resistance		125			0.11	mΩ
V _{TM}	Peak on-state voltage	I _{TM} =5000A, F=78KN	125			1.54	V
dv/dt	Critical rate of rise of off-state voltage	V _{DM} =0.67V _{DRM}	125			1000	V/μs
di/dt	Critical rate of rise of on-state current	V _{DM} =67%V _{DRM} to4000A, Gate pulse t _r ≤0.5μs I _{GM} =1.5A	125			250	A/μs
I _{rm}	Reverse recovery current	I _{TM} =2000A, tp=1000μs, di/dt=-20A/μs, VR=50V	125			250	A
t _{rr}	Reverse recovery time		125			26	μs
Q _{rr}	Recovery charge		125			3250	μC
I _{GT}	Gate trigger current		25	40		300	mA
V _{GT}	Gate trigger voltage	V _A =12V, I _A =1A	25	0.8		3.0	V
I _H	Holding current		125	20		300	mA
V _{GD}	Non-trigger gate voltage	V _{DM} =67%V _{DRM}	125	0.3			V
R _{th(j-h)}	Thermal resistance Junction to heatsink	At 180° sine, double side cooled Clamping force 78KN				0.009	°C /W
F _m	Mounting force			70		85	KN
T _{stg}	Stored temperature			-40		140	°C
W _t	Weight				1900		g
Size	Package box size			160 × 145 × 65			mm

PERFORMANCE CURVES FIGURE

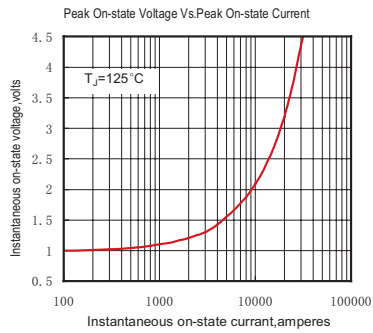


Fig.1

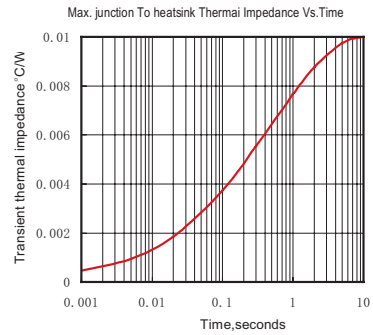


Fig.2

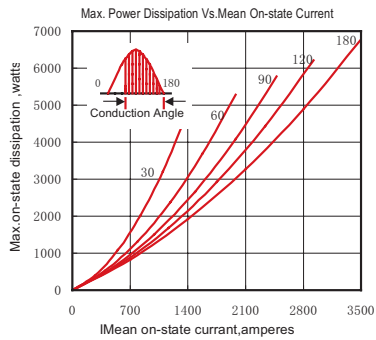


Fig.3

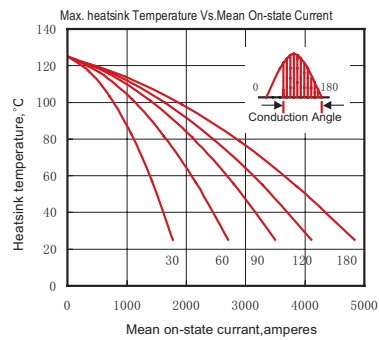


Fig.4

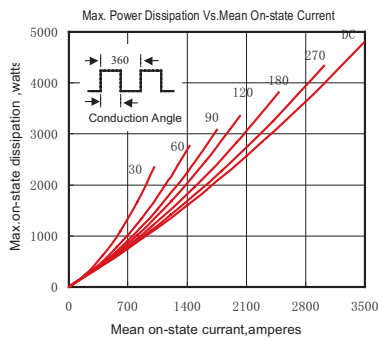


Fig.5

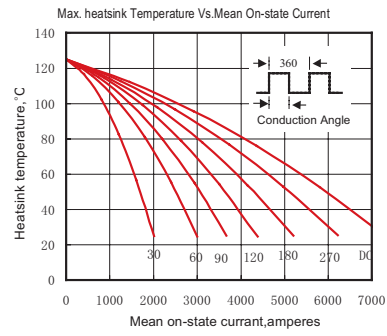


Fig.6

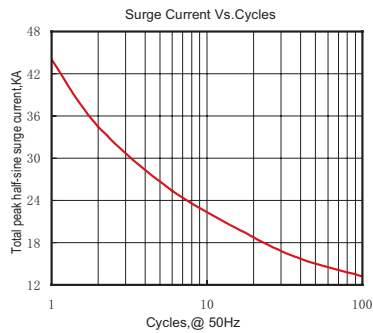


Fig.7

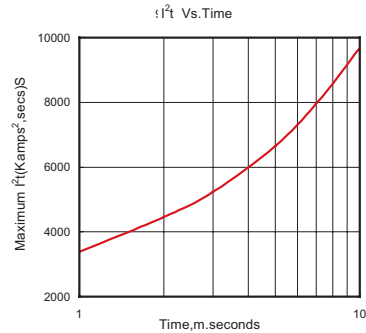


Fig.8

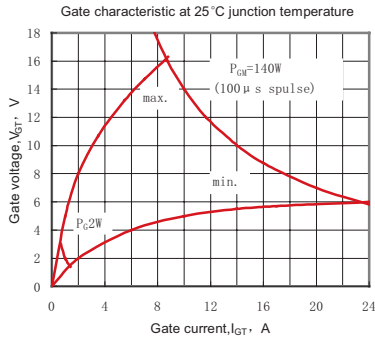


Fig.9

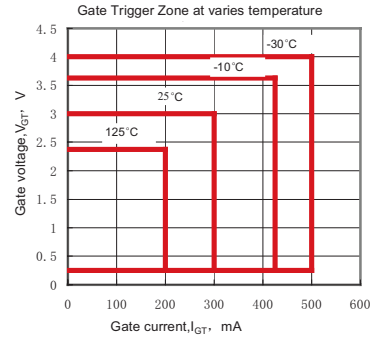
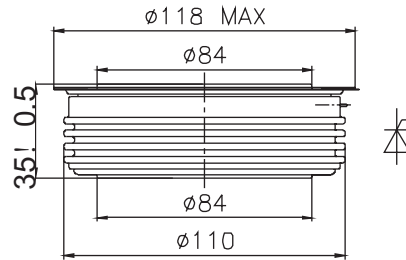
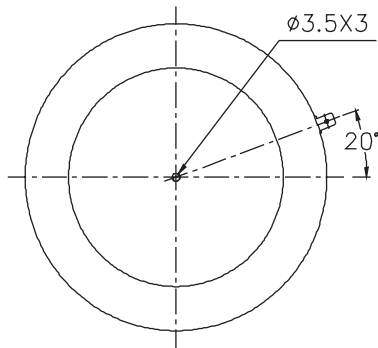


Fig.10

OUTLINE



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